WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a substrate;

a gate oxide film formed on said substrate;

a gate electrode provided on said gate oxide film;

first and second diffusion regions respectively formed in said substrate at each lateral side of said gate electrode;

said gate electrode including a first region located right underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with respective concentrations such that said second region contains N with a higher concentration as compared with said first region.

2. A semiconductor device as claimed in claim 1, wherein said N atoms are distributed in said gate oxide film with a depth profile such that said depth profile has a peak in the vicinity of an interface between said gate oxide film and said substrate.

3. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level

of at least about 0.5%.

4. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level of at least about 1%.

5. A semiconductor device as claimed in claim 1, wherein said gate oxide film contains said N atoms in said second region with a concentration level of at least about 2%.

Subt C'

6. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask.

7. A method as claimed in claim 6, wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing

N atoms.

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8. A method as claimed in claim ~~7~~ 6, wherein said atmosphere contains NO and said thermal annealing process is conducted at a temperature of about 800°C.

Subt C2

9. A method as claimed in claim ~~9~~ 7, wherein said atmosphere contains N_2O and said thermal annealing process is conducted at a temperature of about 900°C.

10. A method as claimed in claim ~~7~~ 6, wherein ~~asid~~ said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions.

11. A method as claimed in claim 10, wherein said ion implantation process is carried out under an acceleration voltage of not exceeding about 10 keV.

12. A method as claimed in claim 10, wherein said ion implantation process is carried out

with a dose of ~~about~~ $1 - 3 \times 10^{14} cm^{-2}$.

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~~13. A method as claimed in claim 6, further comprising the step of forming diffusion regions at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.~~

14. A semiconductor device, comprising:

a substrate;

a gate oxide film formed on said substrate;

a gate electrode provided on said gate oxide film;

side wall layers respectively disposed on each lateral side of said gate electrode;

first and second impurity regions respectively formed in said substrate at each lateral side of said gate electrode, which is substantially aligned the edges thereof;

first and second lightly doped impurity regions respectively formed in said substrate at each outer lateral side of said side wall layers, which is substantially aligned the edges thereof;

said gate electrode including a first region disposed right underneath said gate electrode and a second region adjacent to said first region, said first and second regions containing N atoms with

respective concentrations such that said second region contains N with a higher concentration as compared with said first region.

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